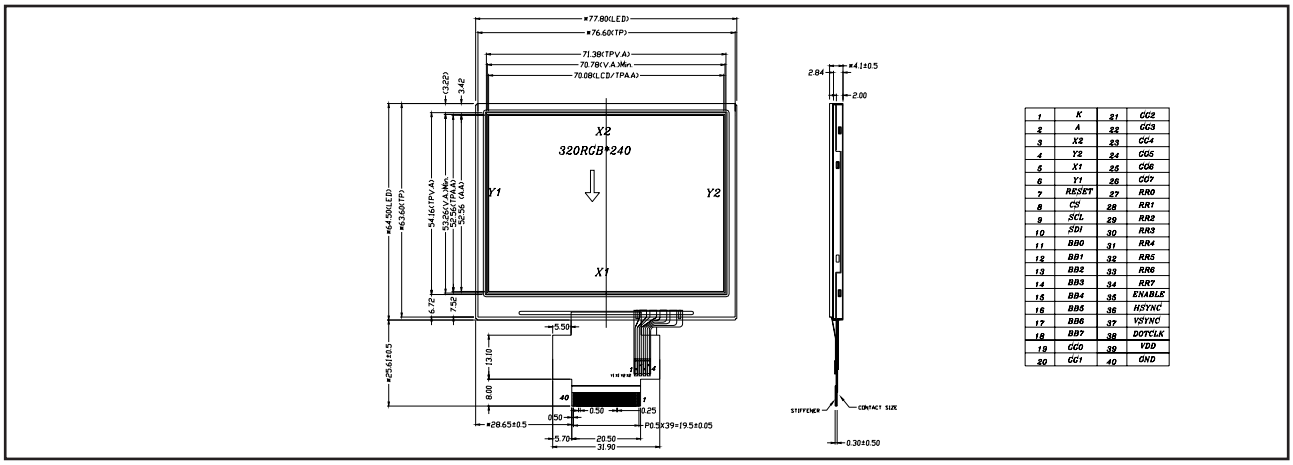
TFT TRANSMISSIVE LCD MODULES

YTS 350ELAK-01-100T

3.5'',320 X 240 DOTS, 1/240 DUTY

EXTERNAL DIMENSION AND DISPLAY PATTERN



1	K	21	CG2
2	A	22	CG3
3	X2	23	CG4
4	Y2	24	CG5
5	X1	25	CG6
6	Y1	26	CG7
7	RESET	27	RR0
8	CS	28	RR1
9	SCL	29	RR2
10	SDI	30	RR3
11	BB0	31	RR4
12	BB1	32	RR5
13	BB2	33	RR6
14	BB3	34	RR7
15	BB4	35	ENABLE
16	BB5	36	HSYNC
17	BB6	37	VSYNC
18	BB7	38	DOTCLK
19	CG0	39	VDD
20	CG1	40	GND

MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H)	77.80 x 64.50 x 4.1	mm
Active Area (W x H)	70.08 x 52.56	mm
Viewing Direction	12:00	o´clock
Number of Dots	320 (RGB) x 240	dots
Colors	16M	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{DD}	-0.3	2.7	V
	V_{DDIO}	-0.3	4.0	V
Input Voltage	V_{CI}	V_{SS}-0.3	5.0	V
Operating Temperature	See page 8			
Storage Temperature				

Note (1): Current Drain per Pin excluding VDD and VSS: 25mA typical.

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	LED_K	LED Backlight
2	LED_A	
3	X_2	The Pin of Touch Panel
4	Y_2	
5	X_1	
6	Y_1	
7	RESET	Reset Pin
8	CS	Chip Select Pin
9	SCL	Clock Pin of Serial Mode
10	SDI	Data Input Pin in Serial Mode
11-18	BB_0-BB_7	Blue Data
19-26	GG_0-GG_7	Green Data
27-34	RR_0-RR_7	Red Data
35	ENABLE	Display Enable Pin from Controller
36	HSYNC	Line Synchronization Signal
37	VSYNC	Frame Synchronization Signal
38	DOTCLK	Dot-Clock Signal and Oscillator Source
39	V_{DD}	Power Supply
40	GND	Ground

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
TFT Gate ON Voltage	V_{GH}			15.0		V
TFT Gate OFF Voltage	V_{GL}	Ta=+25°C		-10.0		V
TFT Common Electrode Voltage	V_{comH} V_{comL}		2.5 -2.0	(3.6) (-2.4)	4.5 0	V

Note (2): V_{com} must be adjusted to optimize display quality: cross talk, contrast ratio and etc.
Note (3): V_{GH} is TFT gate operating voltage.
Note (4): V_{GL} is TFT gate operating voltage. The storage capacitance structure of this products is C_{st} (Storage on Common). The low voltage level of V_{GL} signal must be fluctuated with same phase as V_{com}, in case of Storage on Gate structure.
Note (5): Environmental condition: 25°C±5°C.
Note (6): Operating Voltage V_{CC}=3.3V

BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Forward Voltage	V_f	I_F=20*2mA	9.0	10.2	10.8	V
Forward Current	I_F			20*2		mA
Power Dissipation	P_d	I_F=20*2mA		0.384		W
Reverse Voltage	V_r				3.0	V
Reverse Current	I_r					mA
Luminous Intensity	L_V	I_F=20*2mA	6000			cd/m^2
Luminous Uniformity	ΔL_V		75	80		%
Chromaticity Coordinate	X	I_F=15mA, Ta=25°C each chip	0.27		0.33	
	Y		0.27		0.33	

Note (7): Operating temperature range Topr -30°C to +70°C; Storage temperature range Tsty -40°C to +85°C.

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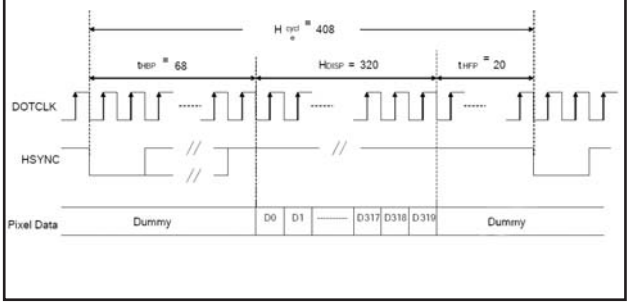
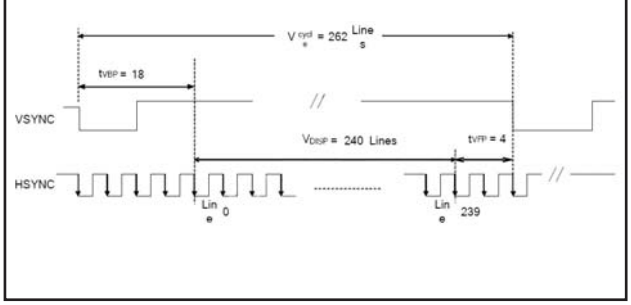
TIMING OF POWER SUPPLY: DATA TRANSACTION TIMING IN PARALLEL RGB (24 BIT) INTERFACE (SYNC MODE)

(a) Horizontal Data Transaction Timing



(a) Vertical Data Transaction Timing



PARAMETER		SYMBOL	MIN.		TYP.		MAX.		UNIT
			24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency		f_{DOTCLK}			6.5	19.5	10	30	MHz
DOTCLK Period			100	33.3	154	51.3			ns
Horizontal Frequency (Line)		f_H			14.9		22.35		kHz
Vertical Frequency (Refresh)		f_V			60		90		Hz
Horizontal Back Porch		t_{HBP}			68	204			t_{DOTCLK}
Horizontal Front Porch		t_{HFP}			20	60			t_{DOTCLK}
Horizontal Data Start Point		t_{HBP}			68	204			t_{DOTCLK}
Horizontal Blanking Period		$t_{HBP} + t_{HFP}$			88	264			t_{DOTCLK}
Horizontal Display Area		H_{DISP}			320	960			t_{DOTCLK}
Horizontal Cycle		H_{CYCLE}			408	1224	450	1350	t_{DOTCLK}
Vertical Back Porch		t_{VBP}			18				Lines
Vertical Front Porch		t_{VFP}			4				Lines
Vertical Data Start Point		t_{VBP}			18				Lines
Vertical Blanking Period		$t_{VBP} + t_{VFP}$			22				Lines
Vertical Display Area	NTSC	V_{DISP}			240				Lines
	PAL				280 (PALM=0)				Lines
	PAL				288 (PALM=1)				Lines
Verical Cycle	NTSC	V_{CYCLE}			262		350		Lines
	PAL				313				Lines

SIGNAL TIMING IN DE MODE