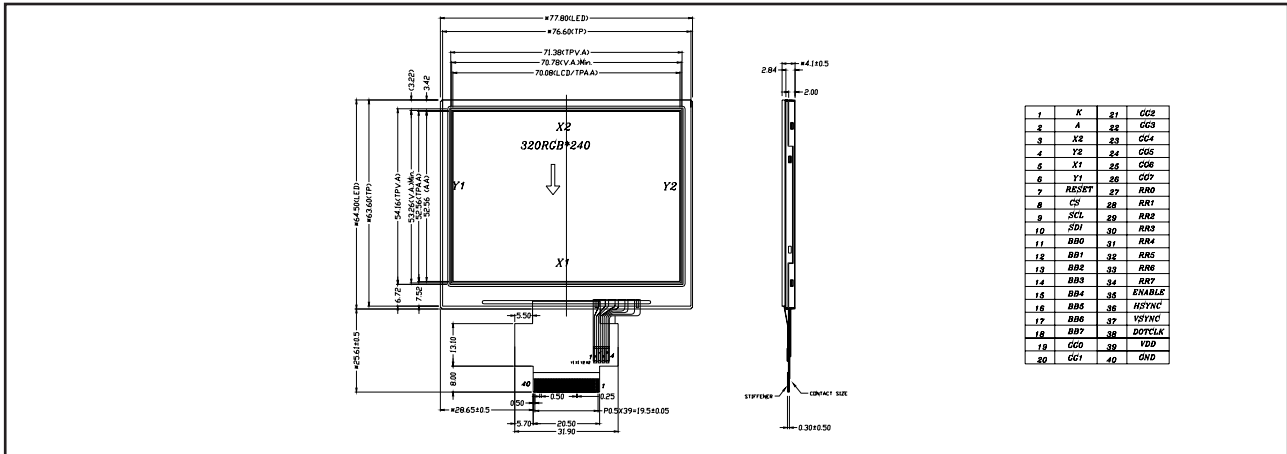


TFT TRANSMISSIVE LCD MODULES YTS 350ELAK-01-100N

3.5", 320 X 240 DOTS, 1/240 DUTY

EXTERNAL DIMENSION AND DISPLAY PATTERN



MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H)	77.80 x 64.50 x 3.04	mm
Active Area (W x H)	70.08 x 52.56	mm
Viewing Direction	12:00	o'clock
Number of Dots	320 (RGB) x 240	dots
Colors	16M	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V _{DD}	-0.3	2.7	V
	V _{DDIO}	-0.3	4.0	V
Input Voltage	V _{CI}	V _{SS} -0.3	5.0	V
Operating Temperature		See page 8		
Storage Temperature				

Note (1): Current Drain per Pin excluding VDD and VSS: 25mA typical.

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	LED_K	LED Backlight
2	LED_A	
3	X ₂ /NC	No Connection
4	Y ₂ /NC	
5	X ₁ /NC	
6	Y ₁ /NC	
7	RESET	Reset Pin
8	CS	Chip Select Pin
9	SCL	Clock Pin of Serial Mode
10	SDI	Data Input Pin in Serial Mode
11-18	BB ₀ -BB ₇	Blue Data
19-26	GG ₀ -GG ₇	Green Data
27-34	RR ₀ -RR ₇	Red Data
35	ENABLE	Display Enable Pin from Controller
36	HSYNC	Line Synchronization Signal
37	VSYNC	Frame Synchronization Signal
38	DOTCLK	Dot-Clock Signal and Oscillator Source
39	V _{DD}	Power Supply
40	GND	Ground

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
TFT Gate ON Voltage	V _{GH}			15.0		V
TFT Gate OFF Voltage	V _{GL}	Ta = +25°C		-10.0		V
TFT Common Electrode Voltage	V _{comH}		2.5	(3.6)	4.5	V
	V _{comL}		-2.0	(-2.4)	0	

Note (2): V_{comH} must be adjusted to optimize display quality: cross talk, contrast ratio and etc.

Note (3): V_{GH} is TFT gate operating voltage.

Note (4): V_{GL} is TFT gate operating voltage. The storage capacitance structure of this products is C_{st} (Storage on Common).

The low voltage level of V_{GL} signal must be fluctuated with same phase as V_{comH} in case of Storage on Gate structure.

Note (5): Environmental condition: 25°C±5°C.

Note (6): Operating Voltage V_{CC}=3.3V

BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

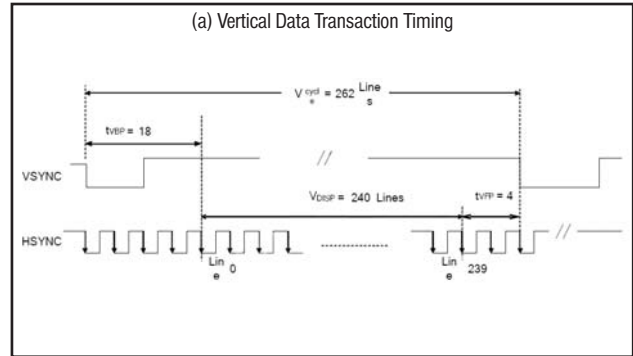
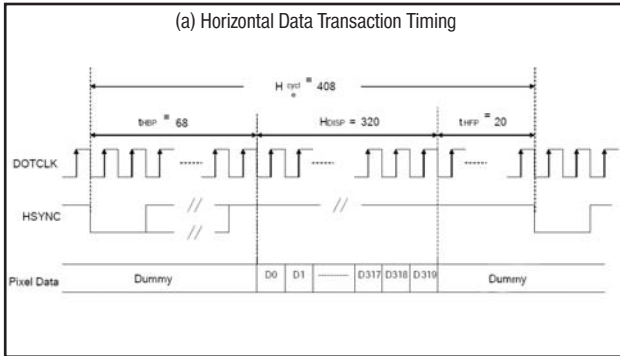
ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Forward Voltage	V _f	I _F =20*2mA	9.0	10.2	10.8	V
Forward Current	I _F		20*2			mA
Power Dissipation	P _d	I _F =20*2mA	0.384			W
Reverse Voltage	V _r					3.0
Reverse Current	I _r					mA
Luminous Intensity	L _v	I _F =20*2mA	6000			cd/m ²
Luminous Uniformity	ΔL _v		75	80		
Chromaticity Coordinate	X	I _F =20mA, Ta=25°C each chip	0.27		0.33	
	Y		0.27		0.33	

Note (7): Operating temperature range T_{opr} -30°C to +70°C; Storage temperature range T_{sty} -40°C to +85°C.

TFT TRANSMISSIVE LCD MODULES YTS 350ELAK-01-100N

3.5", 320 X 240 DOTS, 1/240 DUTY

TIMING OF POWER SUPPLY: DATA TRANSACTION TIMING IN PARALLEL RGB (24 BIT) INTERFACE (SYNC MODE)



PARAMETER	SYMBOL	MIN.		TYP.		MAX.		UNIT
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	f_{DOTCLK}			6.5	19.5	10	30	MHz
DOTCLK Period		100	33.3	154	51.3			ns
Horizontal Frequency (Line)	f_H			14.9		22.35		kHz
Vertical Frequency (Refresh)	f_V			60		90		Hz
Horizontal Back Porch	t_{HBP}			68	204			t_{DOTCLK}
Horizontal Front Porch	t_{HFP}			20	60			t_{DOTCLK}
Horizontal Data Start Point	t_{HBP}			68	204			t_{DOTCLK}
Horizontal Blanking Period	$t_{\text{HBP}} + t_{\text{HFP}}$			88	264			t_{DOTCLK}
Horizontal Display Area	H_{DISP}			320	960			t_{DOTCLK}
Horizontal Cycle	H_{CYCLE}			408	1224	450	1350	t_{DOTCLK}
Vertical Back Porch	t_{VBP}			18				Lines
Vertical Front Porch	t_{VFP}			4				Lines
Vertical Data Start Point	t_{VBP}			18				Lines
Vertical Blanking Period	$t_{\text{VBP}} + t_{\text{VFP}}$			22				Lines
Vertical Display Area	NTSC	V_{DISP}		240				Lines
	PAL			280 (PALM=0)				Lines
	PAL			288 (PALM=1)				Lines
Vertical Cycle	NTSC	V_{CYCLE}		262		350		Lines
	PAL			313				Lines

SIGNAL TIMING IN DE MODE

