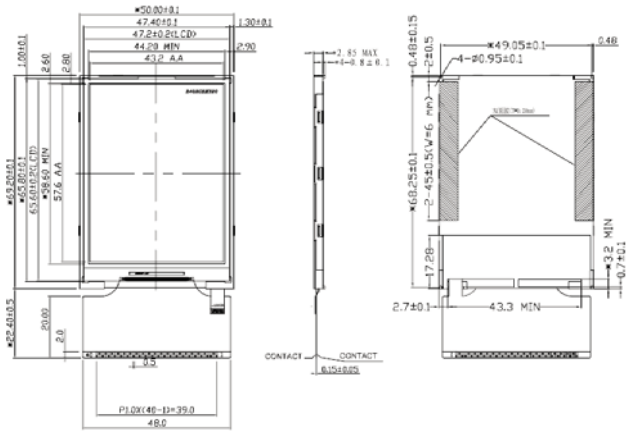
TFT TRANSMISSIVE LCD MODULES

YTS 280DLAC-03-200N

2.8'', 240 X 320 DOTS, 1/320 DUTY

EXTERNAL DIMENSION AND DISPLAY PATTERN



1	LED_K4	21	DB7
2	LED_K3	22	DB6
3	LED_K2	23	DB5
4	LED_K1	24	DB4
5	LED_A	25	DB3
6	P68	26	DB2
7	BS0	27	DB1
8	BS1	28	DB0
9	BS2	29	SDO
10	RESET	30	SDI
11	DB17	31	NRD_E
12	DB16	32	NWR_RNW
13	DB15	33	DNC_SCL
14	DB14	34	NCS
15	DB13	35	VCC
16	DB12	36	GND
17	DB11	37	X1/NC
18	DB10	38	Y1/NC
19	DB9	39	X2/NC
20	DB8	40	Y2/NC

MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H)	50.0 x 69.20 x 2.85	mm
Active Area (W x H)	44.20 x 58.60	mm
Viewing Direction	6:00	o´clock
Number of Dots	240 (RGB) x 320	dots
Colors	262K	
Surface Brightness	160	cd/m^2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage 1	IOV_{CC}	-0.3	4.6	V
Supply Voltage 2	V_{CI}	-0.3	4.6	V
Supply Voltage 3	DDV_{DH}	-0.3	9.0	V
Supply Voltage 4	V_{CL}	-4.6	0.3	V
Supply Voltage 5	V_{GH}	-0.3	18.5	V
Supply Voltage 6	V_{GL}	-18.5	0.3	V
Input Voltage	V_{IN}	-0.3	V_{CI} +0.3	V
Operating Temperature	See page 8			
Storage Temperature				

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	LED_K_4	Backlight LED Power
2	LED_K_3	
3	LED_K_2	
4	LED_K_1	
5	LED_A	
6	P_{68}	Select the MPU Interface Mode
7	BS_0	Select the MPU Interface Mode
8	BS_1	Select the MPU Interface Mode
9	BS_2	Select the MPU Interface Mode
10	RESET	Reset Pin
11-28	DB_{17}-DB_0	Data Bus
29	SD_0	Serial Data Output. If not use, let it to open.
30	SD_I	Serial Data Input Pin
31	NRD_E	I80 System: Serves as a Read Signal and Read Data at the Low Level. M68 System: 0 - Read/Write Disable; 1 - Read/Write Enable. Fix it to IOV_{CC} or V_{SSD} Level when Using Serial Buss Interface.
32	NWR_RNW	I80 System: Serves as a Write Signal and Write Data at the Rising Edge. M68 System: 0 - Write; 1 - Read. Fix it to IOV_{CC} or V_{SSD} Level when Using Serial Buss Interface.
33	DNC_SCL	The Signal for Command or Parameter Select under Parallel Mode
34	NCS	Chip Select Signal
35	V_{CC}	Power Supply
36	GND	Ground
37-40	X_1/NC, Y_1/NC, X_2/NC, Y_2/NC	No Connection

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
TFT Gate ON Voltage	V_{GH}			15.0		V
TFT Gate OFF Voltage	V_{GL}	Ta=+25°C		-8.0		V
TFT Common Electrode Voltage	V_{comH} V_{comL}		2.5 -2.0		4.5 0	V

Note (1): V_{com} must be adjusted to optimize display quality: cross talk, contrast ratio and etc.
Note (2): V_{GH} is TFT gate operating voltage.
Note (3): V_{GL} is TFT gate operating voltage. The storage capacitance structure of this products is C_{st} (Storage on Common). The low voltage level of V_{GL} signal must be fluctuated with same phase as V_{com}, in case of Storage on Gate structure.
Note (4): Environmental condition: 25°C±5°C.
Note (5): Operating Voltage V_{CC}=3.3V

BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Supply Voltage	V_{DD} - V_{SS}		3.0		3.4	V
Supply Current	I_{DD}	fixed		60		µA
Luminance	L_V		3000		5000	cd/m^2
Average	Avg		80			%
Colour Coordinate	X		0.26		0.31	
	Y		0.26		0.31	

Note (6): Operating temperature -20°C to +70°C; Storage temperature -30°C to +80°C.
Note (7): LED - 4 pcs.

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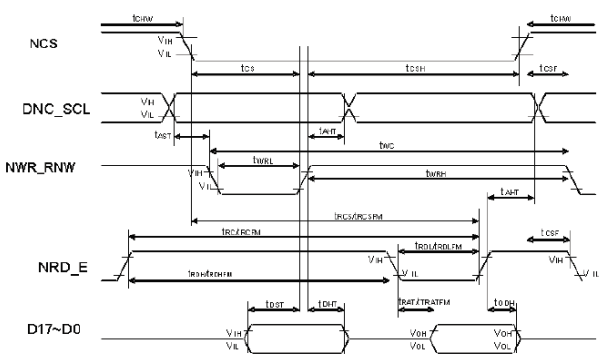
INTERFACE TIMING CHARACTERISTICS

V_{SSA}= 0V, IOCC=1.65V to 2.9V, VCI=2.3V to 2.9V, Ta=-30°C to 70°C

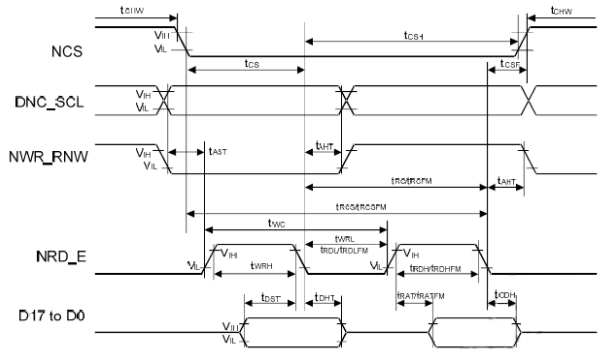
Parallel Interface Characteristics (8080 Series MPU)



PARAMETER	SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Address Hold Time	DNC_SCL	t_{AHT}	Write/Read	10		ns
Address Setup Time		t_{AST}		10		ns
Chip Select „H“ Pulse Width	NCS	t_{CHW}		0		ns
Chip Select Setup Time (Write)		t_{CS}		35		ns
Chip Select Setup Time		t_{RCSFM}		355		ns
Chip Select Wait Time (Write/Read)		t_{CSF}		10		ns
Chip Select Hold Time		t_{CSH}		10		ns
Write Cycle	NWR_ RNW	t_{WC}		100		ns
Control Pulse „H“ Duration		t_{WRH}		35		ns
Control Pulse „L“ Duration		t_{WRL}		35		ns
Read Cycle	NRD_E	t_{RCFM}	When read from GRAM	450		ns
Control Pulse „H“ Duration		t_{RDHFM}		90		ns
Control Pulse „L“ Duration		t_{RDLFM}		355		ns
Data Setup Time	D_{17} to D_0	t_{DST}	for max. C_L=30 pF for min. C_L=8 pF	15		ns
Data Hold Time		t_{DHT}		10		ns
Read Access Time		t_{RATFM}			340	ns
Output Disable Time		t_{ODH}		20	80	ns

Note (1): The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOV_{CC} for input signals.

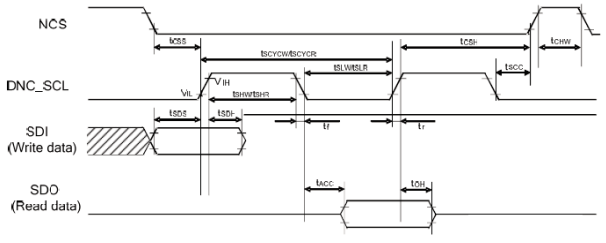
Parallel Interface Characteristics (6800 Series MPU)



PARAMETER	SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Address Hold Time	DNC_SCL	t_{AHT}	Write/Read	10		ns
Address Setup Time		t_{AST}		10		ns
Chip Select „H“ Pulse Width	NCS	t_{CHW}		0		ns
Chip Select Setup Time (Write)		t_{CS}		35		ns
Chip Select Setup Time		t_{RCSFM}		355		ns
Chip Select Wait Time (Write/Read)		t_{CSF}		10		ns
Chip Select Hold Time		t_{CSH}		10		ns
Write Cycle	NWR_ RNW	t_{WC}		100		ns
Control Pulse „H“ Duration		t_{WRH}		35		ns
Control Pulse „L“ Duration		t_{WRL}		35		ns
Read Cycle	NRD_E	t_{RCFM}	When read from GRAM	450		ns
Control Pulse „H“ Duration		t_{RDHFM}		90		ns
Control Pulse „L“ Duration		t_{RDLFM}		355		ns
Data Setup Time	D_{17} to D_0	t_{DST}	for max. C_L=30 pF for min. C_L=8 pF	10		ns
Data Hold Time		t_{DHT}		10		ns
Read Access Time (ID)		t_{RAT}			100	
Read Access Time (FM)		t_{RATFM}			340	ns
Output Disable Time		t_{ODH}		20	80	ns

Note (2): The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOV_{CC} for input signals.

The Serial Interface Characteristics



PARAMETER	SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Senal Clock Cycle (Write)	DNC_SCL	t_{SCYCW}		100		ns
DNC_SCL „H“ Pulse Width (Write)		t_{SHW}		35		ns
DNC_SCL „L“ Pulse Width (Write)		t_{SLW}		35		ns
Data Setup Time (Write)	SDI	t_{SDS}		30		ns
Data Hold Time (Write)		t_{SDH}		30		ns
Senal Clock Cycle (Read)	DNC_SCL	t_{SCYCR}		150		ns
DNC_SCL „H“ Pulse Width (Read)		t_{SHR}		60		ns
DNC_SCL „L“ Pulse Width (Read)		t_{SLR}		60		ns
Access Time		t_{ACC}	SD_0 for max. C_L=30pF, for min. C_L=8 pF	45	100	ns
Output Disable Time		t_{OH}		15	100	ns
DNC_SCL to Chip Select	DNC_SCL, NCS	t_{SCC}		15		ns
NCS „H“ Pulse Width	NCS	t_{CHW}		45		ns
Chip Select Setup Time		t_{CSS}		60		ns
Chip Select Hold Time		t_{CSH}		65		ns

Note (2): The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOV_{CC} for input signals.